REMARKS

Applicant submits an Excess Claim Fee Payment Letter for one (1) additional independent form.

Claims 1-3, 7-8, and 11-24 are all the claims presently pending in the application. Claim 1 is amended to more clearly define the invention. New claim 24 has been added. Claims 1 and 22-24 are independent.

Applicant thanks Examiners Im and Lee for the courtesies extended to the Applicant's representative during a personal interview on July 20, 2004. During the personal interview, Applicant's representative explained that none of the applied references intends to address the objects of the present invention.

Additionally, during the personal interview, Applicant's representative explained that none of the applied references teaches or suggests any relationship at all between the depth of a lightly doped drain region and the thickness of a gate insulation film and/or the thickness of a gate electrode, let alone any motivation to modify the depth of the lightly doped drain region.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Entry of this §1.116 Amendment is proper. Since the Amendments above narrow the issues for appeal and since such features and their distinctions over the prior art of record were

discussed earlier, such amendments do not raise a new issue requiring a further search and/or consideration by the Examiner. As such, entry of this Amendment is believed proper and Applicant earnestly solicits entry. No new matter has been added.

Claims 1-3, 7-8, 11-12, 19, and 22 - 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yamane, et al. reference (U.S. Pat. No. 6,020,229) in view of the Chien, et al. reference (U.S. Pat. No. 6,432,768). Claims 13-18, and 20-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yamane, et al. reference and the Chien, et al. reference and further in view of the Tsao, et al. reference (U.S. Pat. No. 6,143,594).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention, as defined by independent claim 1, is directed to a semiconductor device that includes a plurality of transistors including different gate insulator film in their thickness value. The plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of transistors include lightly doped drain regions. The gate electrode includes an impurity to suppress depletion. The lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

A second exemplary embodiment of the claimed invention, as defined by independent claim 22, is directed to semiconductor device that includes a plurality of transistors having different gate insulator film thickness values. The plurality of types of transistors having

different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The plurality of transistors include a plurality of sidewalls, a first lightly doped drain region, and a second lightly doped drain region. The first lightly doped drain region and the second lightly doped drain region are formed using the plurality of sidewalls and the gate electrode as a mask. The first and second lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

A third exemplary embodiment of the claimed invention, as defined by independent claim 23, is directed to semiconductor device that includesa plurality of transistors having different gate insulator film thickness values with a polysilicon film layer. The plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof. The thickness of the gate insulator film varies based on the amount of deposited gate electrode materials. The plurality of transistors include a plurality of sidewalls, and lightly doped drain regions formed using the plurality of sidewalls and the gate electrode as a mask. The lightly doped drain regions have depths corresponding to the thickness values of the gate electrode and the gate insulator film.

Conventional NMOSFET devices include the same gate electrode as a mask for both the core-purpose MOSFET and the I/O-purpose MOSFET. However, these devices restrict energy (ion) implantation into the lightly doped drain region making it very problematic to dope an impurity to a deep level thus forming shallow lightly doped drain regions with strong electric fields at the drains, which increase breakdown effects and give rise to hot carriers deteriorating

the reliability of the device. (See Page 3, lines 3-8; Page 8, line 20-Page 9, line 5; Page 12, lines 1-10).

In stark contrast, the present invention includes a plurality of transistors with lightly doped drain regions that have depths corresponding to the thickness values of the gate electrode and the gate insulator film. This feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. (See Page 5, lines 1-10; Page 11, lines 8-11; Page 12, lines 1-10 and 20-24; Page 13, lines 1-7; Page 15, line 20-Page 16, line 11; and Figures 3(I)-(L)).

As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance. (See Page 5, lines 7-10; Page 12, lines 11-25).

II. THE PRIOR ART REJECTION

A. The Yamane et al. reference in view of the Chien et al. reference

The Examiner alleges that the Chien et al. reference would have been combined with the Yamane et al. reference to form the claimed invention.

(1) The present invention includes, as a configuration to solve issues, the following core structures: (i) gate insulator film, (ii) gate electrode, and (iii) lightly doped drain region (LDD).

(2) The structure that is disclosed by the Yamane et al. reference makes it possible, as a resistance element, to use a small parasitic capacitance, which is essential to ensure the high-speed operation/high reliability and a thin polysilicon. With this configuration, "process margin

can be increased without increasing the number of manufacturing steps, and defects due to leakage between the resistance element and the underlying substrate can be eliminated so as to ensure the high manufacturing yield." (Col. 3, lines 6-16).

As explained during the July 20, 2004, personal interview, in stark contrast, the object of the present invention is to intend to suppress depletion of a gate electrode by a transistor with a thinner gate insulator film and to suppress hot carriers by a transistor with a thicker gate insulator film. However, the Yamane et al. reference has no intention of the object of the present invention. This can be supported by the fact that the Yamane et al. reference does not disclose a configuration of LDD.

(3) A thickness of a gate electrode and a LDD in the Chien et al. reference is to realize a low resistance of word lines in logic circuits, solve metal contamination issues by simple manufacturing steps, and form memory and logic devices on the same chip (col. 1, lines 23-45).

As a consequence, the Chien et al. reference does not intend, as claimed in this invention, to suppress depletion of a gate electrode by a transistor with a thinner gate insulator film and to suppress hot carriers by a transistor with a thicker gate insulator film. This can be supported by the fact that the Chien et al. reference does not disclose a configuration relating to a difference of a thickness of a gate insulator film.

Therefore, the Yamane et al. reference does not discloses a configuration of a lightly doped drain region while the Chien et al. reference does not disclose the one which relates to differences of a thickness of a gate insulator film. That is, these two references don't have principal three configurations of the present invention, respectively, as stated in (1) - (3) above.

The three configurations in the present invention are for suppressing depletion of a gate electrode by a transistor with a thinner gate insulator film and to suppress hot carriers by a transistor with a thicker gate insulator film. However, the two applied references do not intend the object of the present invention.

Additionally, the objects of the applied references are not the same as the present invention. Therefore, it would be impossible to combine one reference in which an essential configuration of the present invention is deficient with the other reference in which an essential configuration of the present invention is deficient. Hence, as based on the applied references which lack the main configuration of the present invention, Applicant respectfully submits that one of ordinary skill in the art would not have combined the applied references to achieve the present invention.

Further, Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

The Examiner admits that the Yamane et al. reference does not teach or suggest lightly doped drain regions having depths corresponding to the thicknesses of the corresponding gate electrodes and gate insulator films. As explained above, this feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance.

The Examiner alleges that the Chien et al. reference remedies the deficiencies of the Yamane et al. reference.

However, as explained during the July 20, 2004, personal interview, contrary to the Examiner's allegation, the Chien et al. reference does not remedy the deficiencies of the Yamane et al. reference because the Yamane et al. reference does not teach or suggest lightly doped drain regions having depths corresponding to the thicknesses of the corresponding gate electrodes and gate insulator films.

The Examiner cites Figure 1F of the Chien et al. reference which illustrates a first lightly doped drain region 116 for a memory region 110 and a second lightly doped region 132 for a logic region 120 of a substrate 100. The Examiner alleges: "[i]n detail, Fig. 1F of Chien (sic) shows that a thicker gate (112) with a deeper Ldd region (116) and a thinner gate (124) with a shallow Ldd region (134) (sic)." [Applicant notes that the lightly doped drain region is referenced with numeral 132 and not 134 as alleged by the Examiner (see, for example, col. 3, lines 19-20)].

However, nowhere within the Chien et al. reference is there any mention that the Ldd region 116 is deeper than the Ldd region 132. Rather, the specification of the Chien et al. reference is completely devoid of any discussion whatsoever about the depth of the Ldd regions 116 and 132. Therefore, the Examiner's entire argument rests upon the illustrations of Figs. 1E and 1F which does not make it clear that the Ldd region 116 is deeper than the Ldd region 132.

Indeed, the Figures that the Examiner relies upon in an attempt to support the Examiner's allegation that the Chien et al. reference would motivate one of ordinary skill in the art to make

one lightly doped drain region deeper than another makes absolutely no attempt to draw attention to or even to mention that any lightly doped drain region is deeper than another.

Moreover, the independent claims do not only recite that the lightly doped drain regions have depths that correspond to the thicknesses of the gate electrode. Rather, the claims also recite that the depths of the lightly doped drain regions have depths that correspond to the thicknesses of the gate insulating film

In stark contrast, the Chien et al. reference clearly discloses that the first dielectric layer 102 is the same thickness regardless of the depth of implantation of the lightly doped drain regions 116 and 132. Therefore, assuming arguendo that the Examiner is correct that the lightly doped drain regions 116 and 132 have depths that correspond to the thicknessess of the gate electrodes (i.e that the lightly doped drain region 116 is thicker than the lightly doped drain region 132), the Chien et al. reference clearly does not disclose that the depths of the lightly doped drain regions 116 and 132 correspond to the thicknesses of the gate insulator film 102, because the thickness of the gate insulator film 102 is the same thickness.

Further, even assuming arguendo that one of ordinary skill in the art might have noticed that the lightly doped drain region 116 might be deeper than the lightly doped drain region 132 in Fig. 1F of the Chien et al. reference, despite the lack of any attention being drawn to that feature of the illustration, as explained during the July 20, 2004, personal interview, Applicant respectfully submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner.

The Examiner alleges that "[i]t would be obvious that a deeper Ldd region is formed with a thicker gate since the Ldd region of Chien is formed using the gate as a mask (col. 2, line 51 - col. 3, line 20)."

The Examiner continues this line of reasoning in the Examiner's "Response to Arguments" section of the April 21, 2004 Office Action where the Examiner alleges that "it follows that a higher (sic) a gate structure is, the deeper the Ldd region is."

Based upon these statements from the Examiner, the Applicant must assume that the Examiner misunderstands the process by which a lightly doped drain region is formed.

A doped region is formed by implanting an impurity. The amount of impurity that is implanted and the depth of the implantation is based upon the energy level and exposure time of the implantation energy.

A mask is used in an implantation process to protect certain areas from being doped. Just as in the present invention, the Chien et al. reference relies upon the gate electrode to shield the area below the gate electrode from being implanted with an impurity.

The mere presence of a mask has absolutely no effect upon the depth of the impurity implantation. Further, the use of a gate as a mask has absolutely no effect upon the depth of the impurity implantation. Rather, the depth of implantation depends upon the energy level and the exposure time of the implantation energy.

Therefore, contrary to the Examiner's allegation that "[i]t would be obvious that a deeper Ldd region is formed with a thicker gate since the Ldd region of Chien is formed using the gate

as a mask," one of ordinary skill in the art understands that the use of a gate as a mask has absolutely no effect upon the depth of the implantation.

In other words, one of ordinary skill in the art understands that the mere presence of a thicker gate electrode does not result in a deeper lightly doped drain region.

In summary, while the Applicant concedes that the Chien et al. reference discloses using the gate electrode as a mask when forming the lightly doped regions, Applicant respectfully submits that one of ordinary skill in the art would not have been motivated to modify the semiconductor device to provide a deeper lightly doped drain region for the thicker gate electrodes/insulation films than the thinner gate electrodes/insulation films simply based upon the fact that a gate is used as a mask for the lightly doped drain region as alleged by the Examiner.

Further, Applicant hereby incorporates by reference the traversal of the Examiner's rejections that were set forth in the Amendment that was filed on January 9, 2004.

Specifically, Applicant continues to submit that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different matters and problems.

One of ordinary skill in the art who was concerned with being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element as the Yamane et al. reference is concerned with solving would not have been referred to the Chien et al. reference because the Chien et al. reference is directed to the completely different and unrelated problem of having word lines for a logic

circuits that have a sufficiently low resistance without adversely affecting a memory device that is formed on the same chip. Thus, the references would not have been combined by one of ordinary skill in the art.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner.

The Chien et al. reference does not remedy the deficiencies of the Yamane et al. reference. While the Chien et al. reference appears to disclose LDD regions at 116 and 132 in Figs. 1D - 1F, the Chien et al. reference does not teach or suggest that the depths of these LDD regions correspond to the thickness values of the gate electrode and the gate insulator film.

Rather, as explained above, the Chien et al. reference merely discloses that the LDD regions 116 and 132 may be provided to the semiconductor device at col. 2, lines 54-57 and col. 3, lines 17-19.

The Chien et al. reference does not teach that the depths of the LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film.

Indeed, the Chien et al. reference does not teach or suggest any relationship at all between the depth of the LDD regions 116 and 132 and the thicknesses of the gate electrode and the gate insulator film, let alone that the depth of these LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film.

The Examiner alleges that the Chien et al. reference in Fig. 1F appears to disclose a thicker gate 112 with a deeper LDD region 116 and a thinner gate 124 with a shallow Ldd region 132. However, as explained above, even assuming arguendo that the Chien et al. reference

discloses these features, the Chien et al. reference does not mention anything at all regarding any relationship between the depths of the LDD regions 116 and 132 and the thicknesses of the gate electrodes 112 and 124, let alone that the depths of the LDD regions 116 and 132 correspond to the thickness values of the gate electrode and the gate insulator film.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1-3, 7-8, 11-12, 19, and 22-23.

B. The Yamane et al. reference in view of the Chien et al. reference and in further view of the Tsao et al. reference

Regarding claims 13-18, and 20-21, the Examiner alleges that the Chien et al. reference would have been combined with the Yamane et al. reference and further that the Tsao et al. reference would have been combined with the Yamane et al. reference and the Chien et al. reference to form the claimed invention.

Applicant hereby incorporates by reference the traversal of this rejection that was set forth in the Amendment that was filed on January 9, 2004.

Specifically, Applicant continues to submit that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

As explained previously, one of ordinary skill in the art who was concerned with being able to form a resistance element that is thin enough to reduce parasitic capacitance but does not risk having contact holes that penetrate the resistance element as the Yamane et al. reference is

concerned with solving or who was concerned with the problem of having word lines for a logic circuits that have a sufficiently low resistance without adversely affecting a memory device that is formed on the same chip as the Chien et al. reference is concerned with solving would not have referred to the Tsao et al. reference to solve these problems because the Tsao et al. reference is concerned with the completely different and unrelated problem of providing protection against electrostatic discharge in mixed voltage IC chips. Thus, the references would not have been combined, absent hindsight.

Further, Applicant continues to submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

More importantly, the Examiner appears to have completely ignored the Applicant's arguments by failing to respond to the traversal that was provided to the Examiner in the Amendment that was filed on January 9, 2004. Applicant submits that the Examiner is failing to move the prosecution of this matter forward by failing to provide any response at all to the Applicant's traveral.

Rather, the Examiner merely cuts and pastes the rejection from the October 9, 2003 Office Action into the currently outstanding Office Action that was dated April 21, 2004.

The Examiner's cut and pasted rejection continues to allege that one of ordinary skill in the art would have been motivated to modify the semiconductor device that is disclosed in the Yamane et al. reference to include a NMOS device "since an NMOS is most commonly used for

a semiconductor device." However, contrary to the Examiner's allegation, the mere fact that an NMOS device may be commonly used, does not provide a motivation or suggestion to modify the existing structure that is disclosed by the Yamane et al. reference.

As explained previously, it is not sufficient to merely point out the disclosure of a feature in a secondary reference as a basis for making a modification. Rather, in order to establish a *prima facie* case of obviousness the Examiner must provide a motivation to modify the device disclosed in the Yamane et al. reference.

The Examiner's cut and pasted rejection continues to allege that it would have been obvious to one of ordinary skill in the art to modify the semiconductor device that is disclosed by the Yamane et al. reference "in order to obtain proper operating voltages for electrical function of the device."

In other words, the Examiner's cut and pasted rejection continues to allege that the semiconductor device that is disclosed by the Yamane et al. reference does not include "proper operating voltages for electrical function of the device." Thus, the Examiner is contending that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

However, contrary to the Examiner's allegation, the Yamane et al. reference does not teach or suggest that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

Further, none of the other applied references (the Chien et al. reference and the Tsao et al. reference) teaches or suggests that the semiconductor device that is disclosed by the Yamane et al. reference is not operable.

Therefore, contrary to the Examiner's allegations, one of ordinary skill in the art would not have been motivated to modify the semiconductor device that is disclosed by the Yamane et al. reference based upon the disclosure of the Tsao et al. reference in order to make the semiconductor device that is disclosed by the Yamane et al. reference operable.

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention including a depth of the LDD region that corresponds to the thickness values of the gate electrode and the gate insulator film. As explained above, this feature reduces the electric field in the space region and efficiently suppresses the occurrence of a hot carrier and optimizes high-voltage reliability. As a result, the claimed invention provides a semiconductor device with an increased process margin of the gate etching during manufacturing and improved performance.

As explained above, neither of the Yamane et al. and Chien et al. references teach or suggest the feature of a depth of the LDD region that corresponds to the thickness values of the gate electrode and the gate insulator film.

The Tsao et al. reference does not remedy this deficiency.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 13-18 and 20-21.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-3, 7-8, 11-12, 19, and 22-24, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/21/04

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